# HSA6880 Single Channel Isolated Gate Driver with Protection Features

## 1 Features

- Single-channel isolated driver optimized for automotive and industrial applications
- 3.5A source and sink peak output currents
- 100V/ns operating common mode transient immunity
- Typical 90 ns propagation delay
- Less than ±30 ns pulse width distortion
- Integrated IGBT protection functions:
  - IGBT soft shutdown (SSD)
  - Desaturation detection (DESAT)
  - Active Miller current clamp
  - Input-side and output-side under-voltage lockout (UVLO) protection
  - Fault sensing/reporting to the system controller (DESAT and UVLO)
- Dual complementary TTL compatible inputs
- Extended -40 °C to +125 °C temperature range
- Bipolar or unipolar supply operation
- Wide 30 V output supply range
- UL1577 certification and $V_{ISO}$ = 3333 $V_{RMS}$ for 60 seconds
- Automotive AECQ-100 Qualified Grade 1

## 2 Applications

- Automotive OBC and traction inverters
- AC/DC motor drives
- Air-conditioning inverters
- Welding/plasma equipment
- Uninterruptible power supplies
- Battery charging systems
- Auxiliary inverters for HEV and EV
- PV solar inverters and optimizers

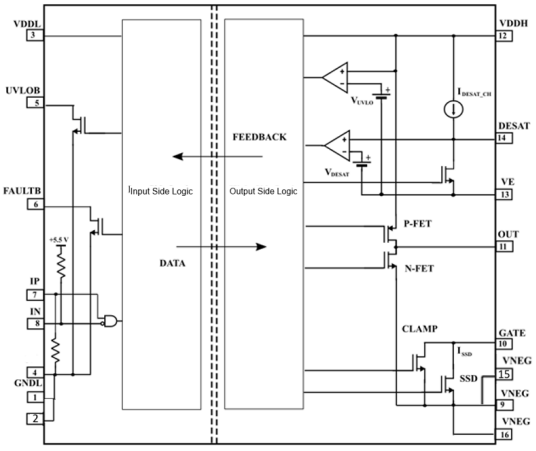


Figure 1 – HSA6880 functional block diagram

## 3 Description

The HSA6880 is a single channel isolated gate driver with complete protection features. It can be used for fast-switching drive and protection of power IGBTs, Si and SiC MOSFETs.The driver incorporates galvanically isolated technology to enable 3333 $V_{rms}$ input-to-output isolation voltage and high transient immunity (100 V/ns) as required in the industrial and automotive applications.

Its short propagation delay and small timing-skew helps to achieve optimum performance at higher switching speeds when compared with other driver solutions available in the market. All logic pins are TTL compatible for easy interface to standard controllers and MCUs.

The HSA6880 architecture complete integrate protection features for protecting the devices in harsh environments. These integrated features include desaturation sensing with soft shutdown protection (also known as soft turn OFF), input-side and output-side under-voltage lockout (UVLO), active Miller current clamping and fault reporting.

The device supports bipolar and unipolar supply voltage configurations. In a bipolar configuration, the driver is typically supplied with voltages of +18V and -5V. For unipolar configuration, the driver is typically supplied with a positive 18 V (max 30 V).

The HSA6880 comes in a SOIC-16 wide-body package to meet UL isolation, creepage and clearance requirement.

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# 4 Pin Configuration

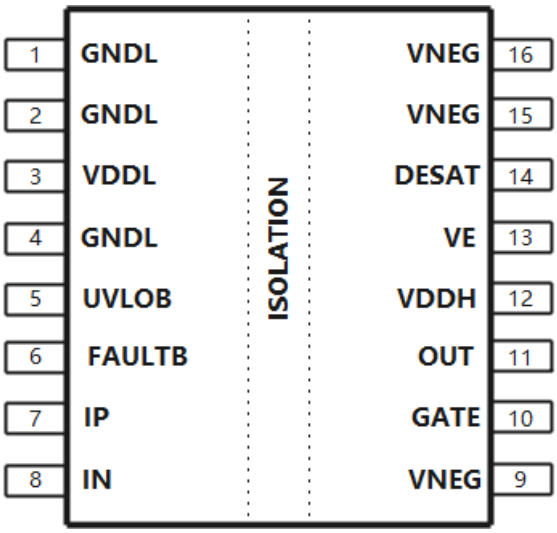



Figure 2 – HSA6880 pin configuration

| PIN | Name | Description |
|---|---|---|
| 1 | GNDL | Input-side ground |
| 2 | GNDL | Input-side ground |
| 3 | VDDL | Input-side power supply |
| 4 | GNDL | Input-side ground |
| 5 | UVLOB | Under-voltage lockout, open drain active LOW output |
| 6 | FAULTB | Desaturation protection fault, open drain active LOW output |
| 7 | IP | Non-inverting driver input [1]. On-chip 120 kΩ pull-down to GNDL |
| 8 | IN | Inverting driver input [2]. On-chip 120 kΩ pull-up to internal 5.5 V supply |
| 9 | VNEG | Output-side negative supply voltage |
| 10 | GATE | IGBT Gate connection for Miller current clamp and SSD (soft shutdown) |
| 11 | OUT | Driver output |
| 12 | VDDH | Output-side positive supply |
| 13 | VE | Supply reference for VDDH and VNEG,connected to IGBT emitter |
| 14 | DESAT | Desaturation (overcurrent protection) sensing input |
| 15 | VNEG | Output-side negative supply voltage |
| 16 | VNEG | Output-side negative supply voltage |

Notes:

1) IP pin controls the IGBT driver output (OUT pin) when IN pin is set to LOW. The IGBT driver is turned ON if IP pin is set to HIGH and IN pin is set to LOW, otherwise, the IGBT driver OUT pin is turned OFF. A minimum pulse width is required to suppress glitches while controlling the IGBT driver. An internal pull-down resistor ensures that the IGBT driver is kept in OFF-state if IP pin is left unconnected.
2) IN pin controls the IGBT driver OUT pin when IP pin is set to HIGH. The IGBT driver is turned ON if IN pin is set to LOW, and is turned OFF if IN pin is set to HIGH. An internal pull-up resistor ensures that the IGBT driver is kept in OFF-state if IN pin is left unconnected.

| Device Information | | | | | |
|---|---|---|---|---|---|
| PART NUMBER | PACKAGE | BODY SIZE | TAPE AND REEL | Device Marking | Comment |
| HSA6880WSRS | SOIC-16 | 10.30 mm × 7.50 mm | Reel | HSA6880-S | Industrial |
| HSA6880WSRQ | SOIC-16 | 10.30 mm × 7.50 mm | Reel | HSA6880-Q | Automotive |

# 5 Specifications

## 5.1 Absolute maximum ratings

Absolute maximum ratings are defined as ratings, which if exceeded, may lead to the destruction of the integrated circuit. Unless otherwise specified, all voltages for input-side and output-side reference to GNDL pin and VE pin respectively.

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input-side supply voltage | VDDL | -0.3 | 30 | V |
| Output-side positive supply voltage | VDDH | -0.3 | 30 | V |
| Output-side negative supply voltage | VNEG | -15 | 0.3 | V |
| Output-side total bipolar supply voltage (VDDH-VNEG) | $V_{MAX\_OUT}$ | | 30 | V |
| OUT voltage | $V_{OUT}$ | VNEG-0.3 | VDDH+0.3 | V |
| OUT peak source current [1] | $I_{OUT\_SOURCE}$ | / | 7 | A |
| OUT peak sink current [2] | $I_{OUT\_SINK}$ | / | 7 | A |
| GATE clamping sink current [3] | $I_{CLAMP\_SINK}$ | / | 2.5 | A |
| Input-side logic levels (UVLOB, FAULTB) | $V_{LOGIC}$ | -0.3 | 5.5 | V |
| Non-inverting driver input voltage | $V_{IP}$ | -0.3 | 5.5 | V |
| Inverting driver input voltage | $V_{IN}$ | -0.3 | 5.5 | V |
| DESAT voltage | $V_{DESAT}$ | -0.3 | VDDH+0.3 | V |
| GATE voltage | $V_{CLAMP}$ | VNEG-0.3 | VDDH+0.3 | V |
| Junction temperature | $T_J$ | -40 | 150 | ℃ |
| Storage temperature | $T_{STG}$ | -55 | 150 | ℃ |
| Operating temperature | $T_A$ | -40 | 125 | ℃ |
| Input-side power dissipation [4] | $P_{D\_IN}$ | | 150 | mW |
| Output-side power dissipation[4] | $P_{D\_OUT}$ | | 520 | mW |

Note:

1) The OUT peak current is measured at maximum pulse width equal to 2.5 µs, maximum duty cycle 1%.
2) The OUT sink current is measured at maximum OFF time equal to 2.5 µs, maximum duty cycle 99%.
3) The GATE clamp sink current is measured at maximum OFF time equal to 2.5 µs, maximum duty cycle 99% and voltage between GATE pin and VNEG pin equal to 2 V.
4) Output IC power dissipation is derated linearly above 100°C from 520 mW to 260 mW at 125°C.

## 5.2 Electro-static discharge

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| ESD – Human Body Model | $V_{ESD\_HBM}$ | / | 4.0 | kV |
| ESD – Charged Device Model | $V_{ESD\_CDM}$ | / | 1000 | V |

## 5.3 Recommended operating conditions

| Parameter | Symbol | Min | TYP | Max | Unit |
|---|---|---|---|---|---|
| Input-side supply voltage | VDDL | 8 | 12 | 18 | V |
| Output-side positive supply voltage | VDDH-VE | 14 | - | 28 | V |
| Output-side negative supply voltage | VNEG-VE | -12 | - | 0 | V |
| Output-side total bipolar supply voltage | VDDH-VNEG | - | - | 28 | V |
| Ambient operating temperature | $T_A$ | -40 | - | 125 | ℃ |
| Input pulse width [1] | $t_{ON}$ | 250 | - | - | ns |

Note:
1) Tested with a load of 10 nF capacitor and a 10 Ω resistor in series.

## 5.4 Electrical characteristics

Unless otherwise specified, all MIN/MAX specification parameters are over the recommended operating conditions, all voltages at input-side are referenced to GNDL pin. All voltages at output-side are referenced to VNEG pin. All typical values are tested at $T_A$ = 25 °C, VDDL = 12 V, VDDH-VNEG = 20 V, VE-VNEG = 0 V.

### 5.4.1 Power supply and UVLO timing

| Parameters | Symbol | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| Input-side current (driver OFF) | $I_{LS\_OFF}$ | | 3.6 | 6.0 | mA |
| Input-side current (driver ON) | $I_{LS\_ON}$ | | 11.4 | 14.5 | mA |
| Output-side current (driver OFF) | $I_{HS\_OFF}$ | | 6.8 | 10 | mA |
| Output-side current (driver ON) | $I_{HS\_ON}$ | | 7.5 | 11 | mA |
| VDDH UVLO threshold voltage (ON) [1] | $VDDH_{UVLO\_H}$ | 11.2 | 12.2 | 13.2 | V |
| VDDH UVLO threshold voltage (OFF) [1] | $VDDH_{UVLO\_L}$ | 10.5 | 11.5 | 12.5 | V |
| VDDH UVLO hysteresis [1] | $VDDH_{UVLO\_HYS}$ | | 0.7 | | V |
| VDDL UVLO threshold voltage (ON) [1] | $VDDL_{UVLO\_H}$ | | 7.5 | | V |
| VDDL UVLO threshold voltage (OFF) [1] | $VDDL_{UVLO\_L}$ | | 7.3 | | V |
| VDDL UVLO hysteresis [1] | $VDDL_{UVLO\_HYS}$ | | 0.2 | | V |
| Minimum duration for UVLOB LOW report [2] | $t_{MIN\_UVLO\_REPORT}$ | | 100 | | μs |
| VDDH UVLO to OUT go low delay [2] | $t_{UVLO\_ON}$ | | 8.8 | | μs |
| VDDH UVLO to OUT go high delay [2] | $t_{UVLO\_OFF}$ | | 8.8 | | μs |
| OUT to UVLOB high low communication delay [2] | $t_{HL\_UVLO\_COM\_DEL}$ | | 1.1 | | μs |
| OUT to UVLOB low high communication delay [2] | $t_{LH\_UVLO\_COM\_DEL}$ | | 1.1 | | μs |

Notes:
1) UVLO is measured with respect to VDDH - VE.
2) Guaranteed by design. (See *Figure 4 to Figure 6* for definition of timing.)

### 5.4.2 Logic inputs and outputs

Test conditions: All typical values at $T_A$ = 25°C; VDDL-GNDL = 12 V; VDDH-VE = 20 V; VNEG-VE = 0 V; -40°C < $T_A$ < 125°C.

| Parameters | Symbol | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| IN current (HIGH = 5 V) | $I_{IN\_H}$ | | 0 | | µA |
| IP current (HIGH = 5 V) | $I_{IP\_H}$ | | 45 | | µA |
| IN current (LOW = 0 V) | $I_{IN\_L}$ | | -50 | | µA |
| IP current (LOW = 0 V) | $I_{IP\_L}$ | | 0 | | µA |
| IN voltage (LOW) | $V_{IN\_L}$ | | | 0.8 | V |
| IN voltage (HIGH) | $V_{IN\_H}$ | 2.4 | | | V |
| IP voltage (LOW) | $V_{IP\_L}$ | | | 0.8 | V |
| IP voltage (HIGH) | $V_{IP\_H}$ | 2.4 | | | V |
| FAULTB, UVLOB current (LOW = 0 V) | $I_{DIG\_LOW}$ | | | 10 | mA |
| Voltage of UVLOB (FAULTB) pin when sinking 10 mA | $V_{DIG\_LOW}$ | | | 400 | mV |

### 5.4.3 Gate Driver output characteristics

Test conditions: All typical values at $T_A$ = 25°C; VDDL-GNDL = 12 V; VDDH-VE = 20 V; VNEG-VE = 0 V; $C_L$ = 100 pF; -40°C < $T_A$ < 125°C.

| Parameters | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| High level output voltage | $V_{OUT\_H}$ | $I_{OUT}$ = -100 mA | | VDDH-0.2 | | V |
| Low level output voltage | $V_{OUT\_L}$ | $I_{OUT}$ = 100 mA | | VNEG+0.1 | | V |
| Peak source output current | $I_{OUT\_SOURCE}$ | $V_{OUT}=V_{DDH}$–18V<br>$C_L$=10nF<br>Single Pulse = 1us | 3.5 | 5.5 | | A |
| Peak sink output current | $I_{OUT\_SINK}$ | $V_{OUT}=V_{NEG}$+18V<br>$C_L$=10nF<br>Single Pulse = 1us | 3.5 | 5.5 | | A |
| Output voltage rise time (10 % to 90%) | $t_r$ | Rg=10 Ω, $C_L$= 10 nF | | 42 | | ns |
| Output voltage fall time (90% to10%) | $t_f$ | Rg=10 Ω, $C_L$= 10 nF | | 32 | | ns |
| Turn ON propagation delay (50% to 50%) | $t_{D\_ON}$ | Rg=10 Ω, $C_L$= 10 nF | | 90 | | ns |
| Turn OFF propagation delay (50% to 50%) | $t_{D\_OFF}$ | Rg=10 Ω, $C_L$= 10 nF | | 90 | | ns |
| Pulse width distortion [1] | PWD | Guaranteed by design | | ±30 | | ns |
| Dead-time distortion [2] | DTD | Guaranteed by design | | ±40 | | ns |
| Common mode transient immunity Logic High [3] | CMTI_LH | | 100 | | | V/ns |
| Common mode transient immunity Logic Low [3] | CMTI_LL | | 100 | | | V/ns |

Notes:
1) Pulse width distortion (PWD) is defined as ($t_{D\_ON}$ - $t_{D\_OFF}$) in any given unit.
2) Deadtime Distortion (DTD) is defined as ($t_{D\_OFF}$ - $t_{D\_ON}$) between any two parts under the same test conditions.
3) $V_{CM}$ = 1200 V.

### 5.4.4 Active Miller clamp and Soft Shutdown

Test conditions: All typical values at $T_A$ = 25°C; VDDL-GNDL = 12 V; VDDH-VE = 20 V; VNEG-VE = 0 V; $C_L$ = 100 pF; -40°C < $T_A$ < 125°C.

| Parameters | Symbol | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| Soft shutdown (SSD) current during fault conditions VGATE–VNEG = 9V | $I_{SSD}$ | | 50 | | mA |
| Clamp threshold voltage | $V_{CLP\_TH}$ | | VNEG+2.0 | | V |
| GATE clamp sink current [1] | $I_{CLP}$ | | 2.0 | | A |
| GATE clamp voltage [2] | $V_{CLP}$ | | VNEG + 0.3 | | V |

Notes:
1) The GATE clamp sink current is measured at $V_{out}$ = VE + 3 V.
2) The voltage is measured at $I_{CLP}$ =100 mA.

### 5.4.5 Desaturation protection

Test conditions: All typical values at $T_A$ = 25°C; VDDL-GNDL = 12 V; VDDH-VE = 20 V; VNEG-VE = 0 V; $C_L$ = 100 pF; -40°C < $T_A$ < 125°C (see Figure 9).

| Parameters | Symbol | MIN | TYP | MAX | Test Conditions | Unit |
|---|---|---|---|---|---|---|
| DESAT threshold voltage | $V_{DESAT\_TH}$ | 6.5 | 7.1 | 7.6 | | V |
| DESAT charging current | $I_{DESAT\_CH}$ | | 0.9 | | $V_{DESAT}$ = 2 V | mA |
| DESAT discharging current | $I_{DESAT\_DSCH}$ | | 110 | | $V_{DESAT}$ = 5 V | mA |
| Initial DESAT blanking time[1, 2] | $t_{DESAT\_BLANKING}$ | | 0.5 | | Guaranteed by design | µs |
| DESAT output mute time [1, 2] | $t_{DESAT\_MUTE}$ | | 3.2 | | Guaranteed by design | ms |
| DESAT to FAULTB low delay [1, 2] | $t_{DESAT\_FAULTB\_LOW}$ | | 4.8 | 7 | Guaranteed by design | µs |
| DESAT to 90% GATE delay [1] | $t_{DESAT\_90\%\_GATE}$ | | 0.3 | | $C_{GATE}$ = 1 nF | µs |
| DESAT to 10% GATE delay [1] | $t_{DESAT\_10\%\_GATE}$ | | 0.8 | | $C_{GATE}$ = 1 nF | µs |
| Off time to reset FAULTB [1, 2] | $t_{DESAT\_FAULTB\_RESET}$ | | 3.2 | | Guaranteed by design | ms |

Notes:
1) See Figure 9 for the DESAT parameters
2) Timing guaranteed by design depends on the clock frequency and can vary ±30%.

### 5.4.6 Insulation Specifications

| Parameters | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| External clearance | CLR | Shortest terminal-to-terminal distance through air | 8.3 | mm |
| External creepage | CPG | Shortest terminal-to-terminal distance across the package surface | 8.3 | mm |
| Distance through the insulation | DTI | Minimum internal gap (Internal clearance) of the insulation | >17 | μm |
| Insulation withstand voltage for 1 min [1] | $V_{ISO}$ | | 3333 | $V_{rms}$ |
| Insulation withstand voltage for 1 sec [1] | $V_{ISO\_1s}$ | | 4000 | $V_{rms}$ |
| Material Group | MG | | I | |
| Pollution degree | | | 2 | |

Note:

1) The driver is treated according UL1577 (Pin 1 through pin 8 are shorted together and pin 9 through pin 16 are shorted together to form a two-terminal device).

### 5.4.7 Package characteristics

| Parameters | Symbol | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| Input-side to output-side resistance [1] | $R_{IN\_OUT}$ | | $10^{12}$ | | Ω |
| Input-side to output-side capacitance [1, 2] | $C_{IN\_OUT}$ | | 1 | | pF |
| Junction to case thermal resistance | $\Theta_{JC}$ | | 40 | | ℃/W |
| Junction to ambient thermal resistance | $\Theta_{JA}$ | | 75 | | ℃/W |

Notes:

1) The IGBT driver is treated as a two-terminal device. Pin 1 through pin 8 are shorted together and pin 9 through pin 16 are shorted together and $V_{IO}$ = 500 V.
2) f = 1 MHz

# 6 Detailed Description

HSA6880 is a single channel, galvanically-isolated, 3.5 A/1200 V IGBT driver in a SOIC16 Wide-Body package. It can be used for the fast switching of power IGBTs, Si and SiC MOSFETs. Basic galvanic isolation is provided on the chip. The HSA6880 architecture includes several control features which protect the IGBT in harsh industrial and automotive environments. These integrated features include IGBT desaturation sensing with soft turn OFF protection, Input-side and output-side under-voltage lockout (UVLO), active Miller current clamping and fault reporting to the system controller.

## 6.1 Power Supplies

Separate power supplies are required for the input-side and output-side due to the input and output of the HSA6880 being galvanically isolated from each other. The input-side power supply is connected to VDDL pin and GNDL pin. The supply voltage can be between 8 and 18 V. The IGBT driver supports bipolar and unipolar supply voltage configurations. For unipolar configuration, VE and VNEG pins are shorted. The IGBT driver is typically supplied by a positive 18 V (max 30 V). In a bipolar configuration, the driver is typically supplied with voltages of VDDH = +18 V, VNEG = -5 V, both with respect to VE.

## 6.2 Input and Output

### 6.2.1 Non-Inverting and Inverting Inputs

There are two possible input modes to control an IGBT driver:

1) Non-inverting mode (IP controls the driver output while IN is set to low).
2) Inverting mode (IN controls the driver output while IP is set to high).

A minimum input pulse width is defined to filter occasional glitches. Any glitch on IP or IN shorter than 40 ns would be ignored.

The truth table for input and output signals is shown below:

| IP | IN | OUT |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

### 6.2.2 Propagation delay and Rise and Fall Times

The timing diagram for rise and fall times and propagation delay are shown below.

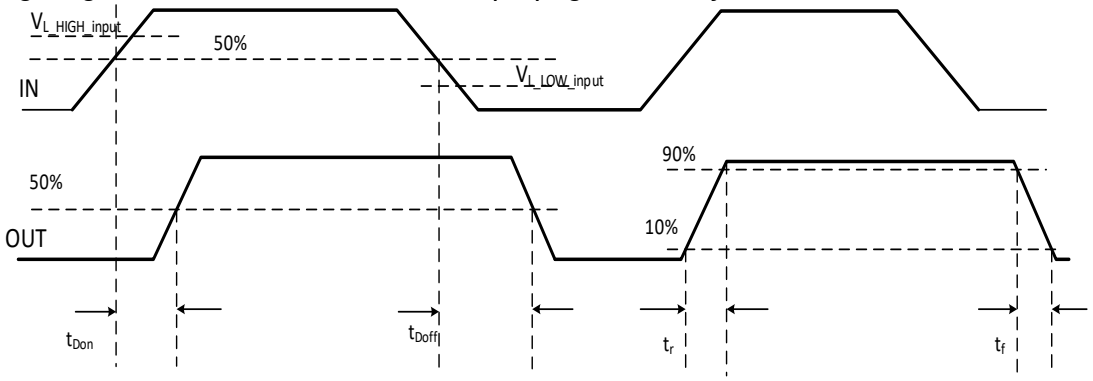



Figure 3 – Propagation delay, and rise and fall times

### 6.2.3 FAULTB and UVLOB outputs

The device has open-drain FAULTB and UVLOB outputs. When the DESAT fault control scheme reports overcurrent conditions of the IGBT, the FAULTB pin transitions from HIGH to LOW. The UVLOB pin transitions to LOW when an UVLO event occurs at the output-side power supply. Pull-up resistors are required on both pins (see Figure 17).

### 6.2.4 Driver output

The driver output section provides a rail-to-rail output, it clamps LOW during faults and under-voltage lockout. During normal operation condition, OUT pin drives the IGBT gate to HIGH or LOW according to the signals applied to IP pin and IN pin. The driver can provide up to 3.5 A sink and source peak currents to charge and discharge the IGBT gate capacitance.

## 6.3 Internal UVLO protection

To ensure correct switching of the power devices, an under-voltage lockout (UVLO) function is integrated in the output-side of the IGBT driver. When the output-side power supply, VDDH falls below $VDDH_{UVLO\_L}$, the IGBT is turned OFF and the input signals at IP pin and IN pin are ignored until VDDH rises above $VDDH_{UVLO\_H}$. The time between UVLO detection until the driver output goes low is “VDDH UVLO to OUT go low delay”, $t_{UVLO\_ON}$. The driver does not turn ON immediately when VDDH rises above $VDDH_{UVLO\_H}$. The time between this event and the turn ON event is called “VDDH UVLO to OUT go high delay”, $t_{UVLO\_OFF}$.

### 6.3.1 Normal UVLO

When an UVLO event happens, a report is sent to the UVLOB pin. The time between the driver output going low to the time UVLOB pin goes low is “OUT to UVLOB high low communication delay”, $t_{HL\_UVLO\_COM\_DEL}$. The time between the driver output going high to the time UVLOB pin goes high is “OUT to UVLOB low high communication delay”, $t_{LH\_UVLO\_COM\_DEL}$.

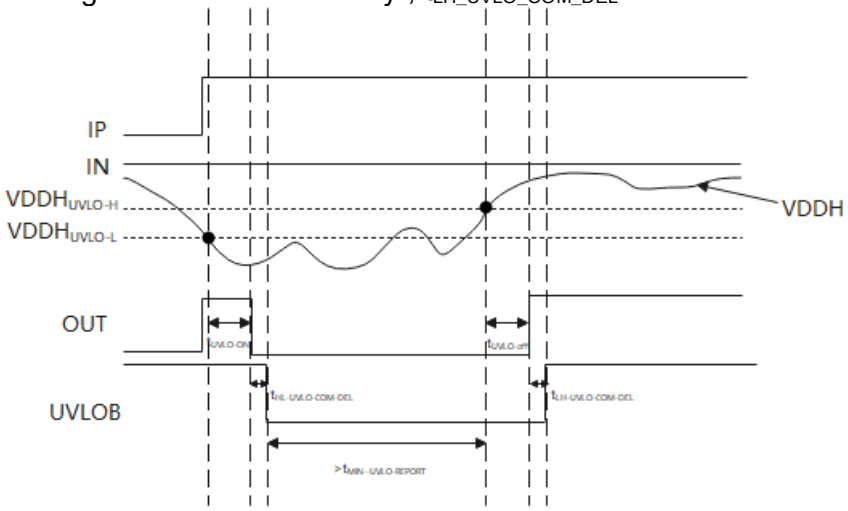



Figure 4 – the HSA6880 during UVLO condition for times higher than $t_{MIN\_UVLO\_REPORT}$.

### 6.3.2 Short UVLO rejection

When VDDH falls below the threshold voltage $VDDH_{UVLO\_L}$ for a time shorter than the time $t_{UVLO\_ON}$, the driver does not turn OFF as shown in

When UVLOB pin is reported and VDDH rises above $VDDH_{UVLO\_H}$, the driver is enabled, and OUT pin goes high only after time $t_{UVLO\_OFF}$. The UVLO pin goes high after the $t_{MIN\_UVLO\_REPORT}$ time and communication delay, $t_{HL\_UVLO\_COM\_DEL}$.

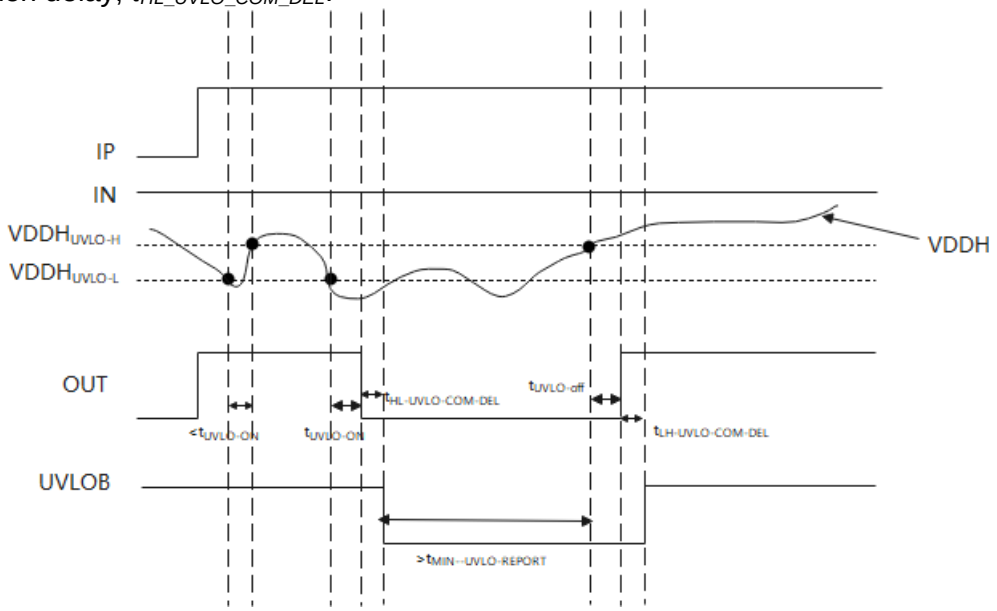



Figure 5 – Short UVLO rejection

### 6.3.3 Unstable VDDH recovery

When the driver is under UVLO condition and VDDH goes high but is not stable, the driver output will not go high until VDDH rises above $VDDH_{UVLO\_H}$ for a time longer than $t_{UVLO\_OFF}$. This is shown in Figure 6.

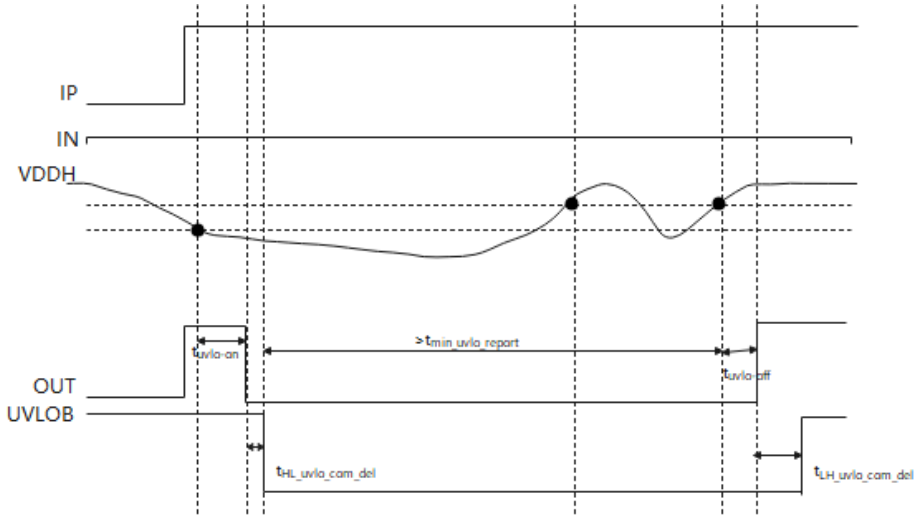



Figure 6 – Unstable VDDH recovery

## 6.4 External Protection

### 6.4.1 Desaturation Protection (DESAT)

The IGBT driver has a DESAT pin for de-saturation protection which monitors the IGBT collector emitter saturation voltage ($V_{CE}$). The DESAT pin is connected to the IGBT collector by a diode, D1, and a resistor R1. The diode blocks the voltage across the IGBT during its OFF state. The diode should be fast to respond to the fault and has minimum reverse recovery to prevent a false trip. For very high IGBT blocking voltages in the kilovolts range, multiple diodes in series could be used. Multiple diodes can also be used to adjust the actual DESAT threshold voltage.

$$V_{DESAT\_TH\_ACTUAL} = V_{DESAT\_TH} - I_{DESAT_{CH}} * R_1 - n * V_F$$

Where n is number of diodes and $V_F$ is a diode forward voltage drop. The time for the driver to respond to DESAT condition is known as blanking time, $t_{DESAT\_BLANKING}$. The blanking time depends on the internal charge current, $I_{DESAT\_CH}$, DESAT reference threshold voltage, $V_{DESAT\_TH}$, and the DESAT capacitor, C5 (see Figure 7). C5 starts to charge with current $I_{DESAT\_CH}$. A zener diode, D2, is placed in parallel with the capacitor C5 to avoid any voltage overshoot between DESAT and VE pins.

When the voltage on DESAT pin becomes higher than $V_{DESAT\_TH}$, soft turn OFF of the IGBT is performed. The capacitor value determines the blanking time $t_{DESAT\_BLANKING}$.

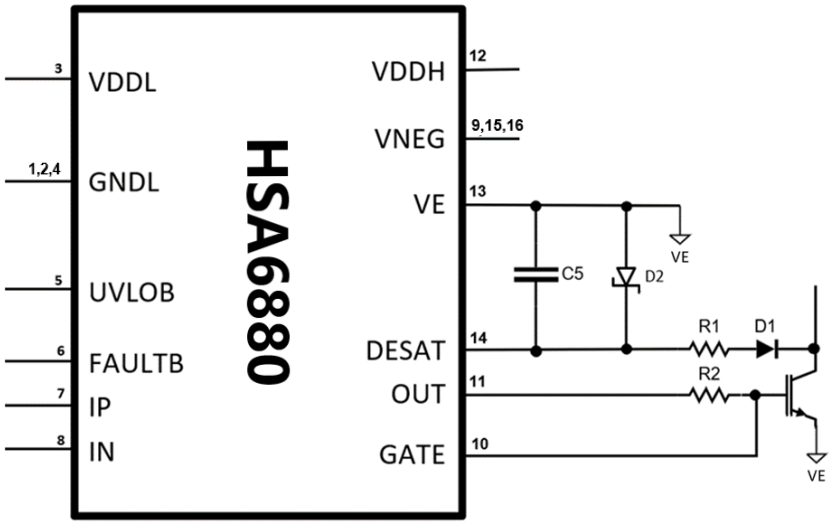



Figure 7 – DESAT circuitry

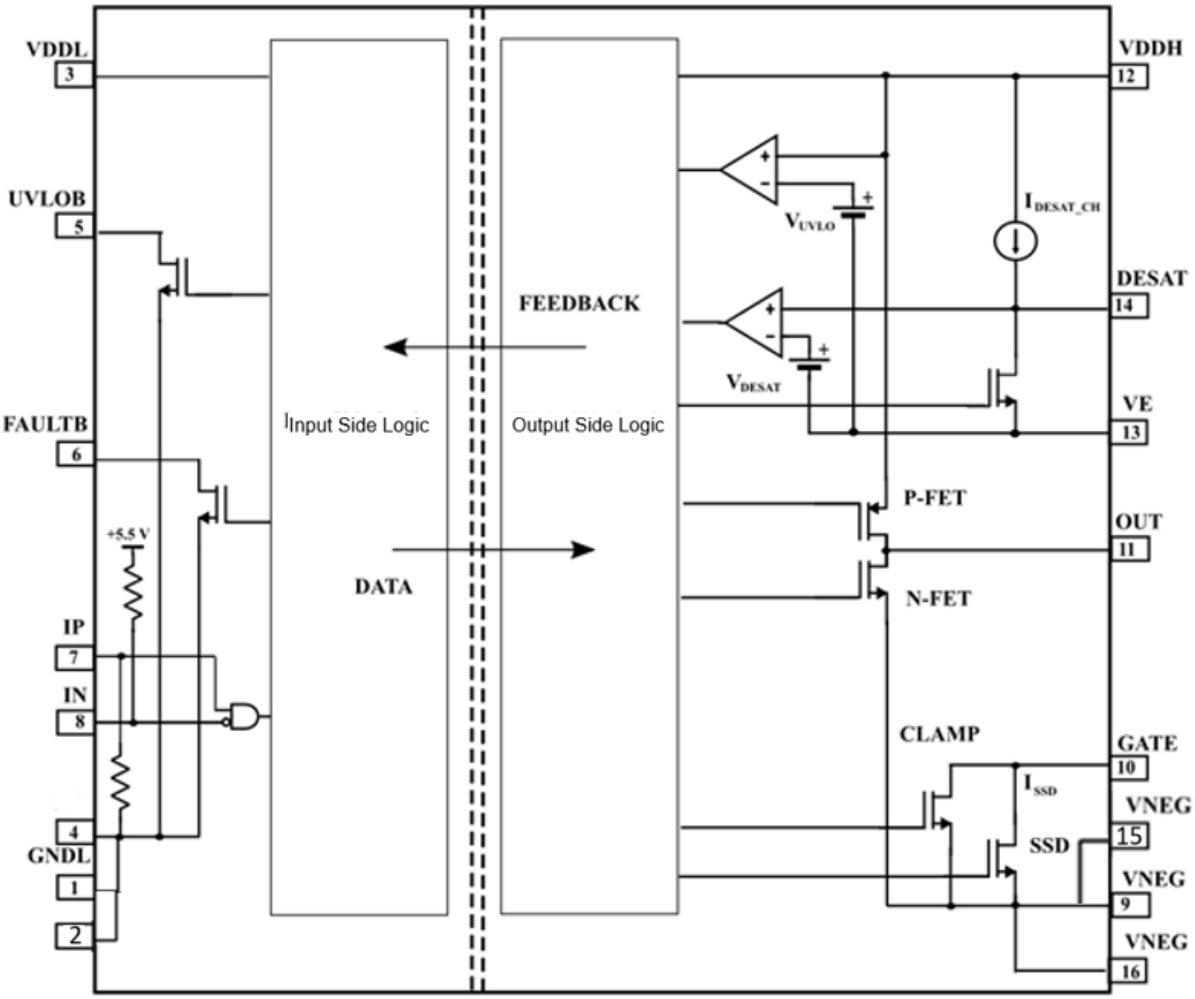



Figure 8 – HSA6880 functional block diagram

The driver time diagram during DESAT conditions is shown in Figure 10. The delay from DESAT sense to starting soft turn OFF is less than 40 ns (typical). The driver input is muted (ignored) for a minimum time, $t_{DESAT\_MUTE}$, which typical value is 3.2 ms. After the muting time has expired, the driver input is expected to stay continuously low for a minimum DESAT fault reset time, $t_{DESAT\_FAULTB\_RESET}$, which typical value is also 3.2 ms. Depend on the driver input, there are three cases when $t_{DESAT\_FAULTB\_RESET}$ will start:

- If the driver input is low at the end of the muting time, $t_{DESAT\_FAULTB\_RESET}$ starts immediately ;
- If the driver input is high at the end of the muting time, $t_{DESAT\_FAULTB\_RESET}$ is started as soon as the input goes low;
- If the driver input toggles high/low during $t_{DESAT\_FAULTB\_RESET}$, then $t_{DESAT\_FAULTB\_RESET}$ is restarted every time the driver input goes low.

The time to discharge the GATE depends on the IGBT input capacitance, gate-source and drain-source voltages, and the soft-shutdown current during fault conditions ($I_{SSD}$), which is typically 50 mA. When the GATE voltage drops to $V_{CLP\_TH}$, the IGBT gate is shorted to VNEG through the following FETs: CLAMP, main N-FET and SSD. When desaturation protection is activated, the FAULTB pin on the input-side goes to LOW. The time from the DESAT sense is detected and setting the FAULTB pin to LOW, $t_{DESAT\_FAULTB\_LOW}$, is 7μs (Max) by design.

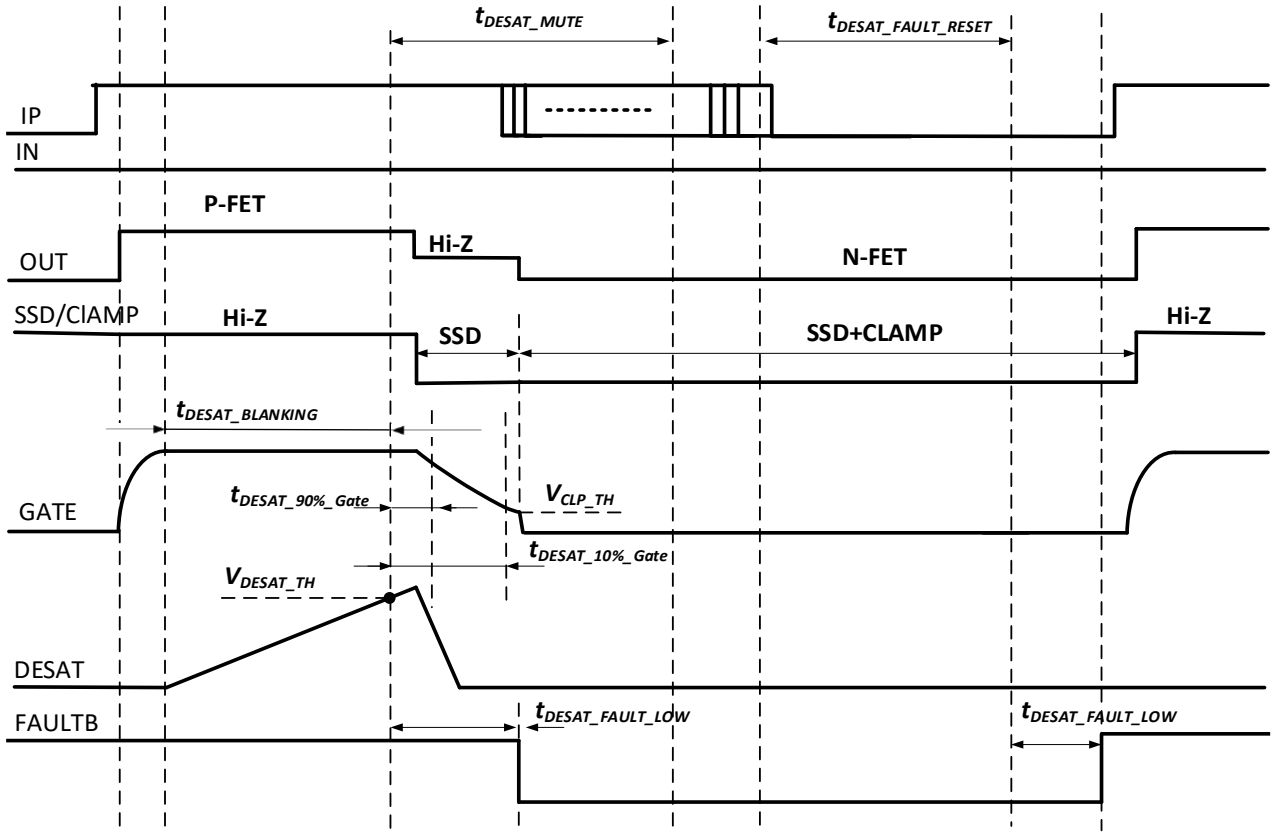



Figure 9 – Driver time diagram during DESAT conditions (the timescale is not proportional)

### 6.4.2 Active Miller clamping

When the IGBT is turned off and the gate voltage drops to the Miller clamp threshold voltage, $V_{CLP\_TH}$, the GATE pin goes from Hi-Z to driving LOW.

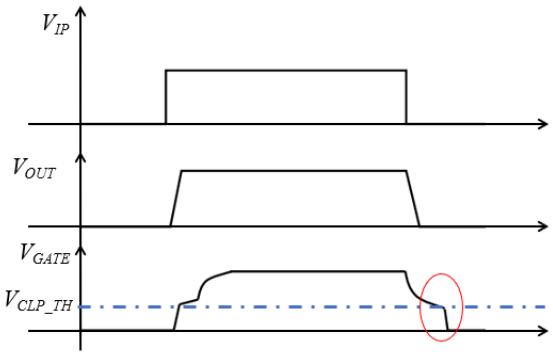



Figure 10 – Voltages on pins IP, OUT and GATE during driver turn ON and OFF

## 7 Isolation

The galvanically isolated barrier in the IGBT driver electrically isolates circuitry between the input-side and the output-side. This barrier prevents unwanted AC or DC signals from traveling from one side to the other.

## 8 Common Mode Transient Immunity

Common mode transient immunity (CMTI) is a key specification parameter of isolated drivers. CMTI is the maximum tolerable rate of the rise or fall of the common mode voltage, $V_{CM}$. HSA6880 is implemented in an advanced Silicon-on-Insulator high-voltage process (SOI) which allows the driver to operate latch-up free (by design), even in the presence of large over/under-shoot voltage excursions. The SOI process allows galvanic separation of internal NFET and PFET devices, preventing the formation of parasitic BJT or thyristors which are the main cause of circuit latch-up. As a result, the driver is immune to the noise generated by large dv/dt and di/dt variations during IGBTs or SiC MOSFETs switching.

## 9 Interlock Protection

The HSA6880 integrates a DEAD-TIME block as an interlock protection function to protect from undesired shoot-through operation. Figure 11 shows the HSA6880 digital top block diagram.

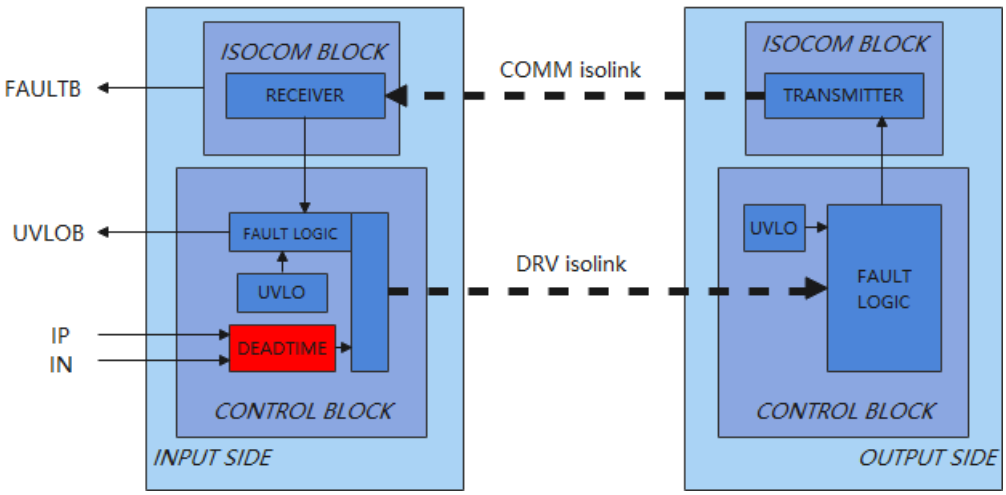



Figure 11 – HSA6880 digital top block diagram

IGBTs are mostly used in three-phase applications such as variable-frequency drives, uninterruptible power supplies, solar inverters, and other similar inverter applications. To ensure proper operation of an inverter, the switches of the inverter leg should not switch simultaneously. A dead-time period is inserted before the transition of output-side and input-side switches to avoid shoot-through.

Figure 13 shows one leg of three-phase converter. Each IGBT has its own driver. When the drivers are connected according to Figure 14, a minimum dead-time of 0.8 µs will be introduced before the switches change state. This feature prevents a shoot-through condition.

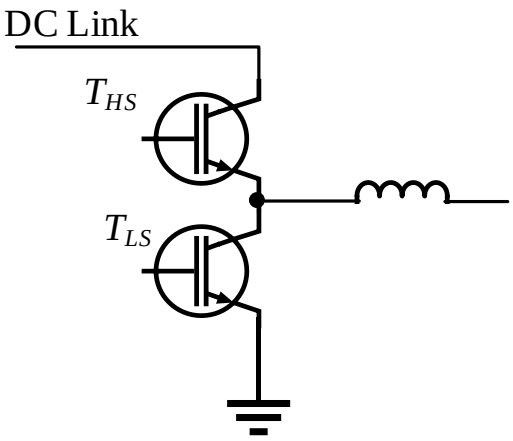



Figure 12 – A leg of three-phase inverter

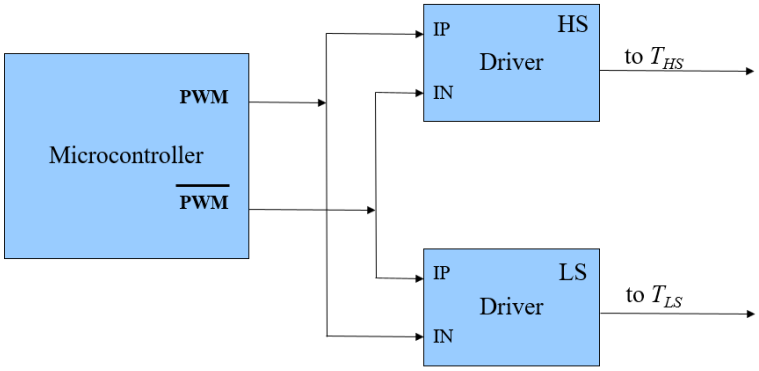



Figure 13 – High and low side drivers connection for interlock protection

Three examples are shown below:

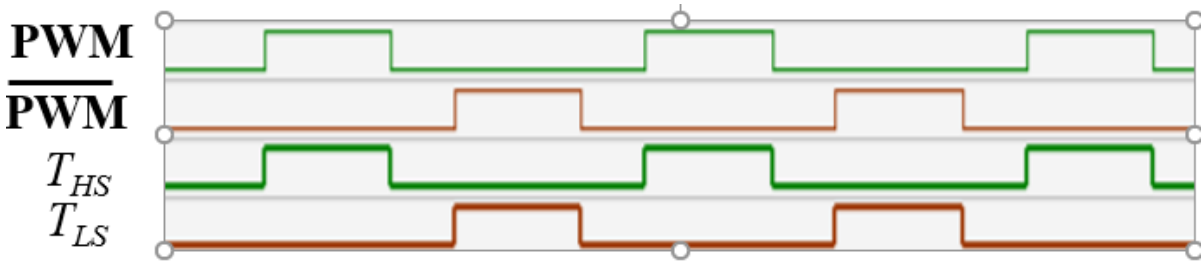



Figure 14 – Driver inputs have enough dead-time.

Original dead-time from the inputs preserved by the driver

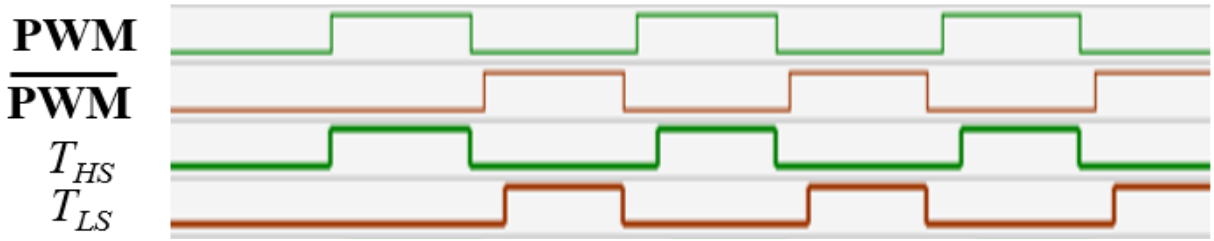



Figure 15 – Driver inputs have some dead-time, but less than the minimum dead-time of the driver. Minimum dead-time ensured by the driver

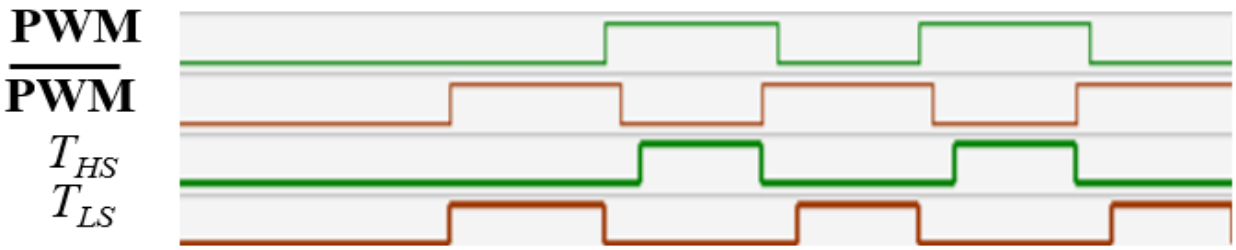



Figure 16 – Driver inputs overlapping.

Minimum dead-time ensured by the driver

## 10 Recommended Application Circuit

Figure 17 shows a recommended application circuit for the IGBT driver.

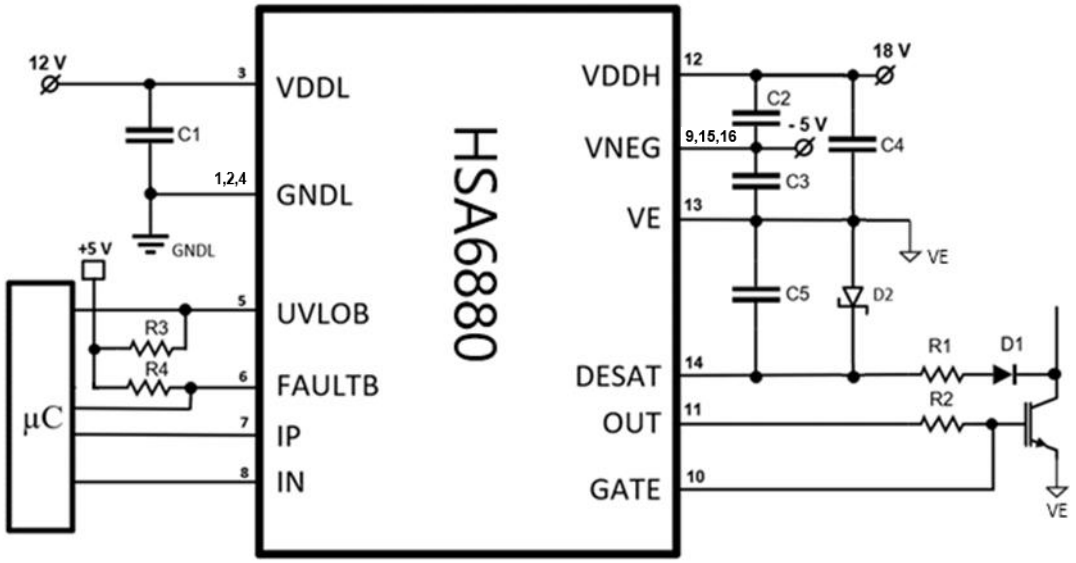
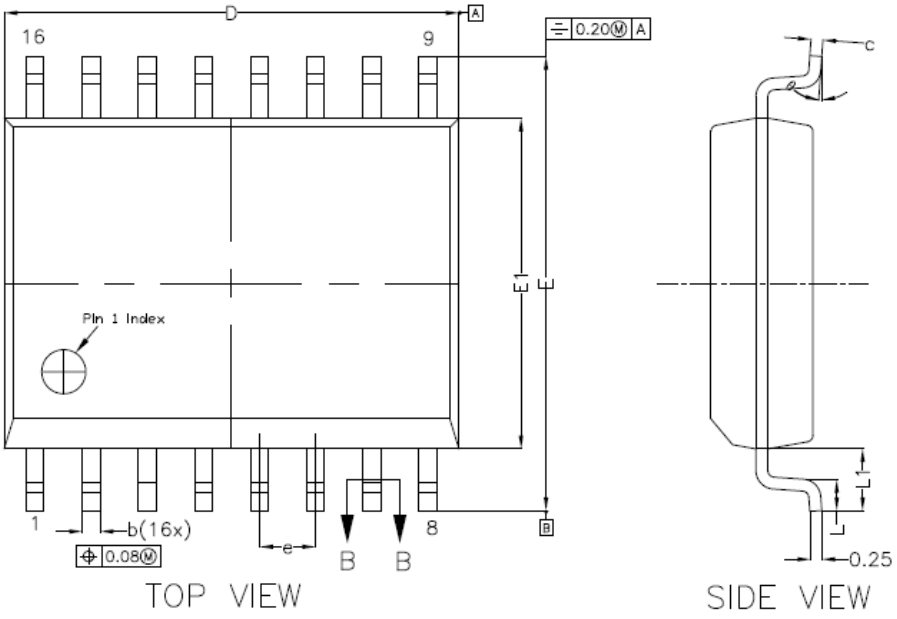


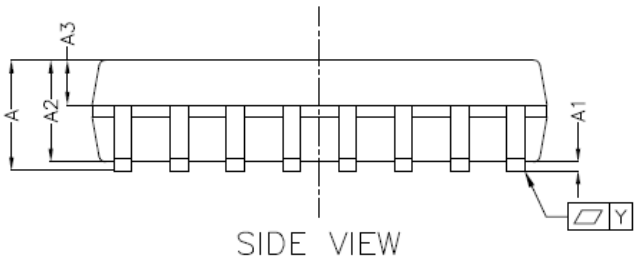

Figure 17 – HSA6880 recommended application circuit

Capacitors C1 and C2 are the decoupling capacitors (recommended value = 1 µF). Capacitors C3 and C4 are decoupling capacitors (recommended value = 10 µF). The DESAT circuit includes a high voltage diode (D1), a 1 kΩ resistor (R1) and 220 pF capacitor (C5). Diode (D2) prevents the voltage on the DESAT pin from falling 0.4 V below the voltage on VE pin.
The gate resistor (R2) limits the gate charge current and indirectly controls the IGBT collector voltage. Its value depends on the IGBT type. A recommended value is 5 Ω.
The pull-up resistors (R3, R4) ensure the input-side outputs are HIGH when no faults are detected. Their recommended value is 3.3 kΩ.

## 11 Package Outline Drawings

The HSA6880 uses a SOIC16 Wide-Body package as shown below:




* CONTROLLING DIMENSION : MM

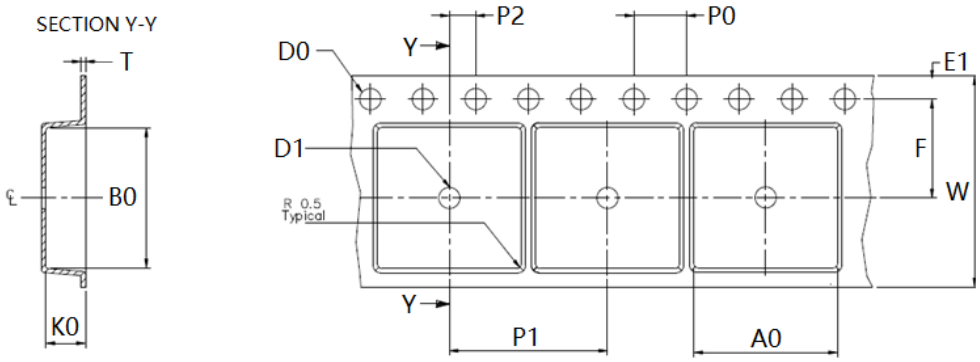
| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | --- | --- | 2.65 |
| A1 | 0.10 | --- | 030 |
| A2 | 2.25 | 2.30 | 2.35 |
| A3 | 0.97 | 1.02 | 1.07 |
| b | 0.35 | --- | 0.43 |
| c | 0.23 | --- | 0.32 |
| D | 10.20 | 10.30 | 10.40 |
| E | 10.10 | 10.30 | 10.50 |
| E1 | 7.40 | 7.50 | 7.60 |
| e | 1.27 bsc | | |
| L1 | 1.40 bsc | | |
| L | 0.55 | --- | 0.85 |
| Y | --- | 0.10 | --- |
| θ | 0° | --- | 8° |

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

## 12 Tape and Reel Dimensions, SOIC16 Wide-Body

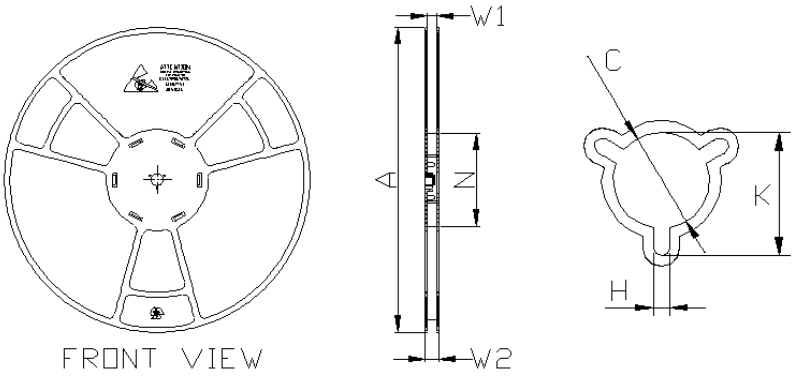
Carrier Tape




UNIT：MM

| PACKAGE | A0 | B0 | K0 | D0 | D1 | W | E1 | F | P0 | P1 | P2 | T |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SOIC16 (Wide-Body) | 10.90 ±0.1 | 10.70 ±0.1 | 3.00 ±0.1 | Ø1.55 ±0.05 | Ø1.60 ±0.1 | 16.00 ±0.3 | 1.75 ±0.1 | 7.50 ±0.1 | 4.00 ±0.1 | 12.00 ±0.1 | 2.00 ±0.1 | 0.30 ±0.05 |

REEL

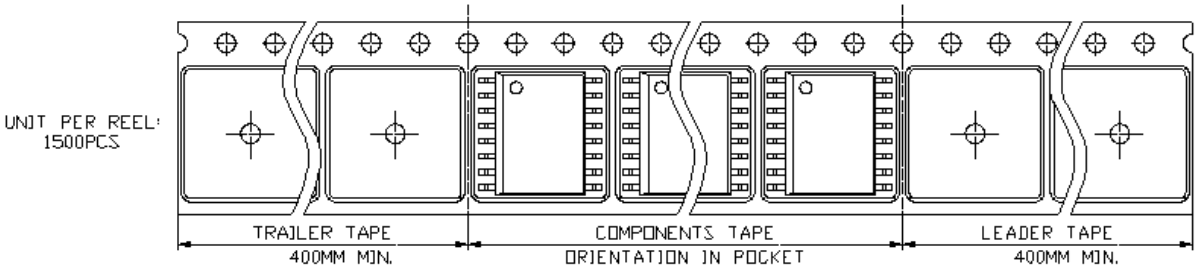



UNIT：MM

| TAPE SIZE | A | N | W1 | W2 | C | K | H |
|---|---|---|---|---|---|---|---|
| 16 MM | Ø330 ± 2 | Ø100 ±2 | 16.4 +2 / -0 | 20.6 +2 / -0 | Ø13.1 ± 0.2 | 16.76 + 0.2 / -0 | 2.1 +0.2 / -0 |

TAPE

Leader / Trailer & Orientation



## Revision History

| Version | Date | Subjects (major changes since previous revision) |
|---|---|---|
| V1.0 | 2021.8.3 | Initial datasheet available |
| V1.1 | 2021.9.10 | 1) Delete "3.5A" from the title<br>2) VDDL limit voltage upper limit is changed from 18V to 30V<br>3) Delete CTI data items<br>4) Delete the word "single" in the DTI data item |
| V1.2 | 2022.3.23 | 1) Page 6 “Common mode transient immunity Logic High” & “Common mode transient immunity Logic Low” is changed from 50 to 100, and the unit is changed from “kV/us” to “V/ns”.<br>2) Page 8 $V_{ISO}$ and $V_{ISO\_1s}$ values update<br>3) Page 4 add “Non-inverting driver input voltage” & “Inverting driver input voltage”, delete the word “(IP and IN)” in “Input-side logic levels”<br>4) Page 14 Figure 9 “Tdeast_BLANKING” update |